Charge offset stability in tunable-barrier Si single-electron tunneling devices

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The problem of charge offset drift in single-electron tunneling (SET) devices can preclude their useful application in metrology and integrated devices. We demonstrate that in tunable-barrier Si-based SET transistors there is excellent stability, with a drift that is in general less than $0.01e$; these devices exhibit some unwanted sensitivity to external perturbations including temperature excursions. Finally, we show that these devices can be "trained" to minimize their sensitivity to abrupt voltage changes. © *2007 American Institute of Physics*.
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The study of solid-state single-electron tunneling devices has been ongoing for about 20 years. The motivations for pursuing such studies include metrology experiments based on the fundamental charge of the electron,[1] quantum computing using charge qubits,[2] and classical computing alternatives including quantum cellular automata.[3] The basic physics of single-electron tunneling (SET) devices is the Coulomb blockade,[4] which is the observation that, for devices with a small enough total capacitance, the charging energy to add one additional electron to the device prohibits charge motion; thus, in these devices, the motion of single electrons can be either monitored or controlled.

The basic circuit element in these devices is a conduction barrier, which is typically a tunnel junction. Much of the early work in this field was with metal-based devices, with a thin metal oxide film serving as the tunnel junction. Recently, SET devices based on complementary metal oxide semiconductor (CMOS)-compatible Si have garnered additional attention;[5] the reasons are as follows: (1) the smaller capacitance in the barriers leads to both faster device operation and larger charging energy (requiring temperatures which are not as low as are necessary in the metal-based devices); (2) the compatibility with CMOS technology makes these devices more easily integrated with existing microelectronic circuitry. An additional motivation for pursuing work in Si-based devices is that of the charge offset: the charge offset refers to a random, time-dependent fluctuation in the operating point of SET transistors (SETTs), due to nonideal fabrication results (in particular, charged defects in the insulating regions of the thin-film devices). In the metal-based devices, a common observation is that the charge offset Q_0 drifts randomly over the time scale of hours or days, thus making it difficult at best to envision integrating these devices.

Several years ago, we demonstrated that in one class of Si-based devices, which have fixed tunnel barriers, the charge offset is constant over long periods of time within about $0.01e$;[6] in contrast, in metal-based devices, the drift can be more than $1e$. Since then, we have been pursuing studies in devices with tunable barriers, which are controlled by small finger gates.[7] Among the advantages inherent in these tunable devices are the increased flexibility of operation and also the excellent homogeneity of devices.[7]

In this letter, we show measurements of the long-term charge offset drift in several tunable-barrier devices. We show that these devices in general have a lack of drift similar to the fixed-barrier devices, although they appear to be somewhat more sensitive to temperature excursions. With the knowledge that these devices have immunity to charge offset drift similar to the previous fixed-barrier ones, workers in the field can continue to pursue the tunable-barrier devices with confidence that the charge offset drift will not be a problem for their operation.

These devices can generally be considered as silicon-on-insulator (SOI) mesa-etched metal oxide semiconductor field effect transistors (MOSFETs) with two layers of gates.[5] The lower gates, which sit directly on the gate oxide of the SOI Si wire, are narrow finger gates that run perpendicular to the wire; by applying voltages to deplete the wire, they provide conduction barriers that form tunnel junctions. The upper gate, which covers both the lower gates and the Si wire, is used to invert the wire and thus provide conduction between the heavily doped source and drain regions. Please see Ref. 7 for more details. Recently, we have shown the excellent homogeneity[7] and a measurement of the "barrier capacitance"[8] in devices nominally identical with the ones in this letter.

Figure 1 shows the basic transistor operation of this SETT. The inset shows the overall dependence on gate voltage; the threshold (near −0.8 V) is very similar to a standard MOSFET. The oscillations are due to the Coulomb blockade behavior,[4] one period corresponds to one extra electron on average in the Si wire. The main part of the curve shows a narrow range of the gate voltage. In order to measure the charge offset as a function of time, we repeatedly measure

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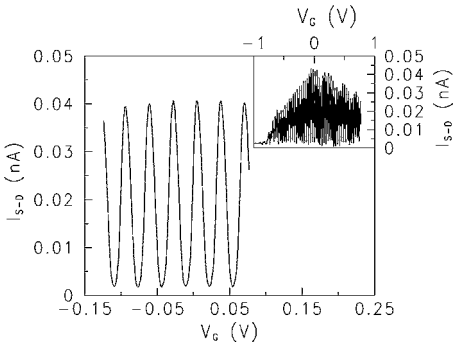

FIG. 1. Current $I_{S\text{-}D}$ vs gate voltage V_G. Inset: large range of gate voltages, showing the turn-on of this transistor, and then a large number of periods of Coulomb blockade modulation. Main: narrow range of gate voltages, corresponding to the region in which the charge offset Q_0 was derived. Note the excellent periodicity of the oscillations in this range. Device AF-CA2R3C-2, T=20–40 mK; bias voltage of 0.6 mV. Zimmer-PC:C/Neil/Papers/06_9 Q0 tunable/Plots/2.48/do_ivg.plot.

these oscillations while holding all other gate voltages fixed; we numerically fit a sinusoidal function to these data, and from the phase of that fit we derive the charge offset in units of e.

Figure 2 shows the derived charge offset as a function of time (over about 2 weeks) from many repeated curves of the type shown in the previous figure; these measurements use a sawtooth-shaped gate voltage for each sweep, which entails a

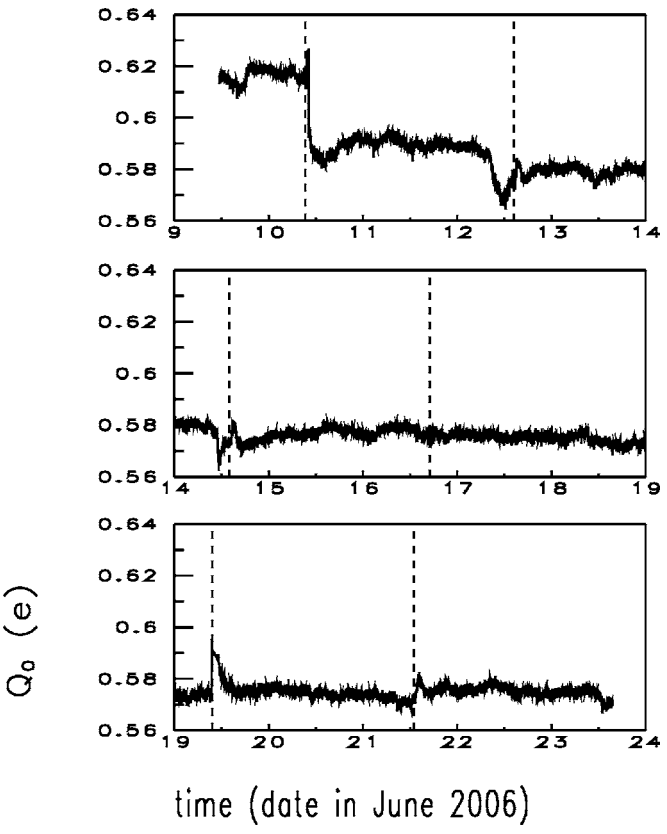

FIG. 2. Charge offset Q_0 vs time for the same device as in Fig. 1, over a period of 14 days. Vertical dashed lines correspond to transfers of liquid helium, which can be a substantial mechanical perturbation of the measurement system. We note that the first transfer, at about 10.4 days, caused a 0.03e change to Q_0. Other than this change, over the subsequent 11.5 days, the charge offset was constant within 0.01e. Device AF-CA2R3C-2, T=20–40 mK. Zimmer-PC:C/Neil/Papers/06_9 Q0 tunable/Plots/2.48/do_q_t_panel_2.48.plot.

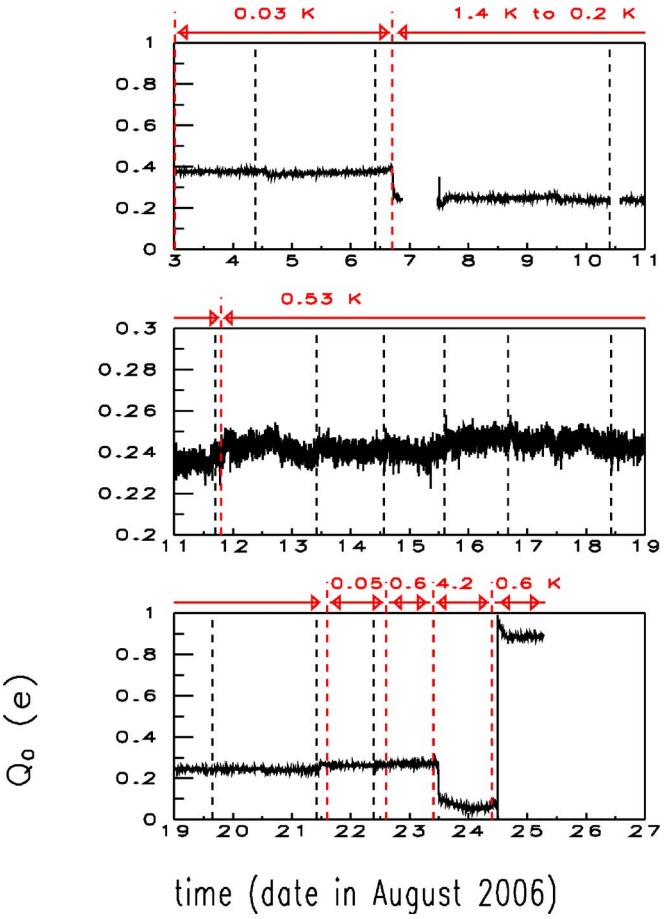

FIG. 3. (Color online) Charge offset vs time for a different device, over a period of 22 days. Black vertical dashed lines indicate transfers of liquid helium, none of which caused any apparent change in Q_0. Note that the middle panel has a different vertical axis, to show a finer scale. For this device, there were quite a number of temperature changes over various periods of time as indicated; changes between stable temperature required about 2 h, so the positions of the lines are uncertain by that amount (about 0.1 day). During the period from about 6.7 to about 11.7 days, the temperature varied between 1.4 and 0.2 K, with a generally downward trend. We note that, in contrast to our previous work on fixed-barrier devices, there is sometimes a nonreproducible change of Q_0 when an abrupt temperature change occurs. This occurred twice, at 6.7 days and at 24.4 days. Note that other abrupt temperature changes, namely, at 11.7, 21.6, and 22.6 days all did not result in a measurable change. Device AF-CA2C3C-3. Zimmer-PC:C/Neil/Papers/06_9 Q0 tunable/Plots/2.51/do_q_t_panel_2.51.plot.

repeated abrupt V_G change of 0.2 V. This graph demonstrates both the similarities and differences with our previous work on fixed-barrier devices.[6] The similarity is exemplified over the 11 day period after 12.5 days: the charge offset varies by less than 0.01e over this entire time period. The differences are demonstrated in the data of the first few days: there are what appear to be two hysteretic, nonreproducible changes in the charge offset, coincident with liquid helium transfers, with a total change of about 0.04e. We note that changes of this size would not appreciably alter the device operation, and so may be acceptable.

Figure 3 shows similar data from a different, nominally identical, device. Again, the data show the similarities and differences with the fixed-barrier devices.[6] The similarity is evident over the 15 day period from 6.7 to 21.5 days, during which the charge offset is constant within 0.012e; this stability occurred even though there were multiple temperature excursions. The difference is evident in the two places, as indicated in the caption, where there were hysteretic, nonre-

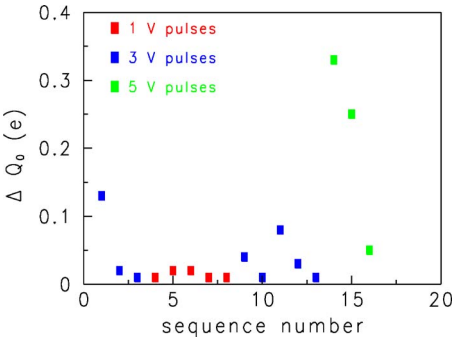

FIG. 4. (Color online) Measurement of hysteretic, nonreproducible changes in charge offset with large gate pulses, for a third device. Typically, several pulses were applied between 0 V and the noted voltage over a few seconds. ΔQ_0 in general was both positive and negative; we have taken the absolute value to provide a clearer graph. This graph shows "training," in that the device becomes more stable upon repeated pulses. In particular, we note that (1) ΔQ_0 becomes generally smaller upon repeated application of both 3 and 5 V pulses; (2) ΔQ_0 was very small for all of the 1 V pulses, because they were preceded by larger 3 V pulses. Device AF-CA2R3D-1, $T=0.02-1.0$ K. Zimmer-PC:C/Neil/Papers/06_9 Q0 tunable/Plots/2.47/do_delta_q_pulsing_2.47.plot.

producible abrupt changes in Q_0 coincident with abrupt changes in the temperature.

In Fig. 4, we show the effect of "training." In general, when we apply large voltage pulses, we can sometimes see hysteretic changes in Q_0. We can see from the figure that, in general, repeated applications of pulses with the same amplitude result in smaller ΔQ_0. Also, we note that in the previous work (which has a very similar result),[6] previous larger pulses made the response to subsequent smaller pulses much smaller; we believe that in Fig. 4, the smallness of the response to the 1 V pulses subsequent to the 3 V pulses (unfortunately, not also measured before the 3 V pulses) corresponds to the same effect. Both of these observations indicate a promising result: we anticipate that we can use these devices in circuits which may require large gate voltages, by first training the devices.

We can thus characterize the charge offset stability of these devices as follows:

(1) In general, the drift when all experimental parameters are held fixed is less than $0.01e$.
(2) These devices have some sensitivity to abrupt external changes, including temperature excursions and possibly mechanical perturbations (liquid helium transfers).
(3) These devices can be trained to minimize the effect of application of large gate voltages.

As discussed above, the charge offset behavior in these tunable-barrier devices is quite similar to the fixed-barrier devices that we previously investigated.[6] However, their sensitivity to abrupt external changes may indicate that they are slightly less robust. While we do not know the cause of this apparent sensitivity, we can list some of the possibly relevant differences between the two classes of devices:

(1) The tunable-barrier devices have an extra layer of lower gates, and also an extra layer of isolation oxide. The extra gates are made of polycrystalline Si, and so the extra isolation oxide may be of different quality than the thermal oxide on single-crystal Si.
(2) Electrostatically, the barriers in the tunable-barrier devices are quite wide (tens of nanometers) but quite low in energy (tens of meV). In contrast, the barriers in the fixed-barrier devices are generally narrower but higher in energy.
(3) Since the tunable-barrier devices have multiple extra gates, there are many more voltages applied to these devices than to the fixed-barrier ones. Fluctuations in these voltages (especially abrupt ones) could lead to or enhance fluctuations in Q_0.[9]

In summary, we have shown the stability of the charge offset in tunable-barrier Si-based SET transistors. In general, the charge offset is quite stable, in the absence of external perturbations. This stability can be enhanced by a training process. Thus, in contrast to previous concerns, the substantially enhanced flexibility of these devices does not result in an enhanced instability in their operation.

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[1] *Recent Advances in Metrology and Fundamental Constants*, edited by Mark W. Keller, In T. J. Quinn, S. Leschiutta, and P. Tavella (IOS, Amsterdam, 2001), Vol. CXLVI, p. 291.
[2] Y. Nakamura, Yu. A. Pashkin, and J. S. Tsai, Nature (London) **398**, 786 (1999).
[3] G. L. Snider, A. O. Orlov, I. Amlani, X. Zuo, G. H. Bernstein, C. S. Lent, J. L. Merz, and W. Porod, J. Appl. Phys. **85**, 4283 (1999).
[4] Hermann Grabert and Michel H. Devoret, *Single Charge Tunneling* (Plenum, New York, 1992).
[5] Yasuo Takahashi, Yukinori Ono, Akira Fujiwara, and Hiroshi Inokawa, J. Phys.: Condens. Matter **14**, R995 (2002).
[6] Neil M. Zimmerman, William H. Huber, Akira Fujiwara, and Yasuo Takahashi, Appl. Phys. Lett. **79**, 3188 (2001).
[7] Akira Fujiwara, Hiroshi Inokawa, Kenji Yamazaki, Hideo Namatsu, Yasuo Takahashi, Neil M. Zimmerman, and Stuart B. Martin, Appl. Phys. Lett. **88**, 053121 (2006).
[8] Neil M. Zimmerman, Akira Fujiwara, Hiroshi Inokawa, and Yasuo Takahashi, Appl. Phys. Lett. **89**, 052102 (2006).
[9] Generally, abrupt or high-frequency noise can more efficiently induce noise than low-frequency fluctuations; in this context, we note that four of the leads had low-pass filters at room temperature, 4 K, and at the base temperature, and two of the leads (upper gate and drain) had only the room-temperature filters. These filters typically have cutoffs at about 10 GHz.